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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/086,871

03/04/2002

Takumi Yamaguchi

60188-456

1896

7590

03/13/2006

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EXAMINER

NGUYEN, LUONG TRUNG

ART UNIT

PAPER NUMBER

2612

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/086,871

Applicant(s)

YAMAGUCHI ET AL.

Examiner

LUONG T. NGUYEN

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 March 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-12 is/are rejected.
- 7) ☒ Claim(s) 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03/04/2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The information disclosure statements (IDS), which are submitted on 03/04/2002, 06/10/2002, 09/27/2002, 03/30/2005 and 06/03/2005 have been considered by the examiner.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-4, 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ihara et al. (JP 10-093070) in view of Gowda (US 6,115,066).

Regarding claims 1, 6, Ihara discloses a solid state image sensor (solid state camera, see Abstract, figure 10, paragraph [0008]) comprising a plurality of amplifying unit pixels arranged two-dimensionally on a semiconductor substrate, each of said plurality of amplifying unit pixels including a photoelectric conversion region (photodiode 115a, figure 10, paragraph [0008]) for subjecting incident light to photoelectric conversion; a read transistor (address transistor 117a,

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figure 10, paragraph [0008]) for reading signal charge obtained through the photoelectric conversion; a storage region (detecting element, which corresponds to floating diffusion FD, figure 10, paragraph [0008]) for storing said signal charge read by said read transistor; a detect transistor (magnification transistor 114a, figure 10, paragraph [0008]) for detecting said signal charge on the basis of application of potential of said storage region to a gate thereof; a reset transistor (reset transistor 116a, figure 10, paragraph [0008]) for resetting said signal charge stored in said storage region; and a drain region (drain line 112, figure 10, paragraph [0008]) for supplying a pulse voltage to said storage region through said reset transistor,

Ihara et al. fail to specifically disclose wherein said drain regions of said plurality of amplifying unit pixels are connected to different drain lines row by row, and said drain line is pulse driven to be set to a HIGH level potential at least during a period when said signal charge stored in said storage region is reset and a period when said signal charge stored in said storage region is detected.

However, Gowda et al. teaches a CMOS image sensor, in which the drain regions VR of plurality pixels 30 are connected to different drain lines 34i row by row (figures 3, 4); and voltage level VR on bus line 34 (drain region) is set high during a period when charge in node 25 is transferred to column bus 15j (figures 4, 6, column 4, line 34 to column 5, line 8, column 6, lines 5-36). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device in Ihara et al. by the teaching of Gowda et al. in order to reduce the size of a pixel of an image sensor. This reduces the size of the image sensor.

Regarding claim 2, Gowda et al. discloses wherein said drain line is set to a HIGH level

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potential during a period when said read transistor is in an ON state (VR is high when charge from node 25 read out to bus 15j, figures 4, 6).

Regarding claim 3, Gowda et al. discloses a vertical shift register for selecting one row of said plurality of amplifying unit pixels; and a circuit for supplying, to said drain line on a corresponding row, a power pulse generated by using an output from one stage of said vertical shift register (timing and control logic 14, figure 3, column 4, line 1 to column 5, line 8).

Regarding claim 4, Gowda et al. discloses a shift register for selecting one row or column of said plurality of amplifying wherein each of said unit pixels, plurality of amplifying unit pixels is driven by a pulse used for driving said shift register (timing and control logic 14, figure 3, column 4, line 1 to column 5, line 8).

Regarding claim 7, Gowda et al. discloses wherein said drain line is set to a HIGH level potential, for the purpose of removing unnecessary charge read from said photoelectric conversion region, during a period when said unnecessary charge is stored in said storage region and a period when said unnecessary charge stored in said storage region is reset (column 6, line 54 to column 5, line 20).

Regarding claim 8, Gowda et al. discloses wherein said drain line is set to a HIGH level potential, for the purpose of removing unnecessary charge read from said photoelectric

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conversion region to said storage region, during a period when both of said read transistor and said reset transistor are turned on (column 6, line 54 to column 5, line 20).

Regarding claim 9, Ihara et al. discloses wherein said drain line is made from the same interconnect layer as that used for forming gates of said read, detect and reset transistors (figures 7, 10).

Regarding claim 10, Ihara et al. discloses wherein a line for connecting said storage region to a gate of said detect transistor is made from a first light blocking metal layer (paragraph [0039]).

Regarding claim 11, Ihara et al. discloses wherein said detect transistors of said plurality of amplifying unit pixels are connected to different signal lines column by column (magnification transistors 114a, 114b, 114c on each column are connected to each signal line 111, figure 10, paragraph [0008]), a line for connecting said storage region to a gate of said detect transistor and said drain line are made from a first metal layer (paragraph [0039]).

Regarding claim 12, Ihara et al. discloses wherein said detect transistors of said plurality of amplifying unit pixels are connected to different signal lines column by column (magnification transistors 114a, 114b, 114c on each column are connected to each signal line 111, figure 10, paragraph [0008]), a line for connecting said storage region to a gate of said detect transistor and said drain line are made from a first metal layer (paragraph [0039]), and said

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drain line is made from a second metal layer above said first metal layer, and said drain line is made from a second metal layer above said first metal layer (figures 10-11).

***Allowable Subject Matter***

5. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Akimoto et al. (US 4,809,075) discloses solid-state imaging device having an amplifying means in the matrix arrangement of picture elements.

Koizumi et al. (US 6,650,369) discloses image sensing apparatus, signal detection apparatus, and signal accumulation apparatus.

Hashimoto (US 6,734,906) discloses image pickup apparatus with photoelectric conversion portion arranged two dimensionally.

Sakurai et al. (US 6,850,278) discloses solid-state image pickup apparatus.

Harada (US 6,707,495) discloses solid-state imaging device and a method of reading a signal charge in a solid state imaging device which can reduce smear and can provide an excellent image characteristic.

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7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to LUONG T. NGUYEN whose telephone number is (571) 272-7315. The examiner can normally be reached on 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID L. OMETZ can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LN  
03/05/06



**LUONG T. NGUYEN**  
**PATENT EXAMINER**